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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,329	02/06/2002	John F. Gilsdorf	TRA-064	3149
36822	7590	08/28/2006	EXAMINER	
GORDON & JACOBSON, P.C. 60 LONG RIDGE ROAD SUITE 407 STAMFORD, CT 06902			MAIS, MARK A	
			ART UNIT	PAPER NUMBER
			2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/072,329	Applicant(s) GILSDORF ET AL.	
	Examiner Mark A. Mais	Art Unit 2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4,5,7-10,13 and 14 is/are rejected.
- 7) ☒ Claim(s) 2-3, 6, 11-12, and 15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4-5, 7-10, and 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Gorshe et al. (USP 6,667,973).

3. With regard to claim 1, Gorshe et al. discloses a system for transferring synchronous and asynchronous signals between broadband access devices, said system comprising:

(a) at least two bus users [**Fig. 1b, HSUs (high speed units), LSUs (low speed units); col. 4, lines 1-4**] ;

(b) a data bus coupled to said at least two bus users [**Fig. 1b, data buses are A Bus, B and C bus, B' and C' bus; col. 5, lines 55-60 and 64-67**];

(c) a clock bus coupled to said at least two bus users [**Fig. 1b, system timing bus is coupled to the HSUs directly, and coupled to the LSUs via HSU; the timing bus is coupled**

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to LSUs because this solves the problem of high/low bus partition which requires different timing units (STUs) driving the clock bus during byte “nibbles”, col. 7, lines 60-61 and col. 8, lines 1-3; *see also* Fig. 1a, PCM control signal 104 includes a global PCM bus clock, col. 6, lines 10-11] ; and

(d) at least one control line coupled to said at least two bus users [Fig. 1b, intra-shelf common control bus, col. 3, lines 60-64; *see also* Fig. 1a, PCM control signal 104 includes per-bus byte status and global SONET send/receive signals, col. 6, lines 10-13], wherein

data is transferred between said at least two bus users over said data bus according to a repeating bus frame having a plurality of slots [STS-1 frames, col. 6, lines 13-15], at least some of said plurality of slots being associated with asynchronous data streams [the data bus carries TDM (synchronous) STS-1 traffic and ATM cells (asynchronous) col. 11, lines 12-18] and said at least one control line being asserted when valid data from one of said asynchronous data streams appears in a slot of said repeating bus frame [the LSU is interpreted as asserting the first control line; byte status signals (such as PRSTAT and PXSTAT) are sent from each LSU (via Fig. 1a's PCM control signal 104, col. 6, lines 10-13) wherein each LSU gets two clock cycles to request to transmit an ATM cell, col. 11, lines 31-33; the HSU receives the request and, as the bus master, allows the LSU to transmit (inherently signaled via Fig. 1a's PCM control signal 104, col. 6, lines 10-13), col. 11, lines 39-42].

4. With regard to claim 4, Gorshe et al. discloses that the at least one control line includes a start of frame indicator which is asserted at the first slot of said repeating bus frame [Fig. 5, the byte status signal (sent via PCM control signal 104, col. 6, lines 10-13) indicates the beginning-

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of-cell on the first slot of the 106 clocks per cell slot necessary to transmit a 53 byte ATM cell (via the data bus), col. 11, lines 25-30].

5. With regard to claim 5, Gorshe et al. discloses that at least one of said asynchronous data streams includes a repeating data frame **[the frame format for transporting synchronous and asynchronous data on the data buses is the STS-1 frame, col. 6, lines 13-15]**, and the at least one control line includes a data frame indicator which is asserted when a slot in said repeating bus frame includes a start of frame indicator for said repeating data frame **[inherently, byte status signals such as PRSTAT and PXSTAT indicate that ATM cells are be transported over the data bus in the STS-1 frame format]**.

6. With regard to claim 7, Gorshe et al. discloses that one of said at least two bus users is coupled to a SONET network and another of said at least two bus users is coupled to a non-SONET network **[Fig. 1b, HSUs are interfaced to SONET high speed interfaces (col. 3, lines 9-16) while LSU is interfaced with low speed (and, therefore, non-SONET) interfaces]**.

7. With regard to claim 8 and 9, Gorshe et al. discloses that either of the HSU or LSUs can be the bus master **[col. 11, lines 39-42]**.

8. With regard to claim 10, Gorshe et al. discloses a method for transferring synchronous and asynchronous signals between broadband access devices, said method comprising:

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(a) generating a repeating bus frame having a plurality of slots **[the frame format for transporting synchronous and asynchronous data on the data buses is the STS-1 frame, col. 6, lines 13-15];**

(b) associating at least some of said slots with asynchronous data streams **[the data bus carries TDM (synchronous) STS-1 traffic and ATM cells (asynchronous) col. 11, lines 12-18] ;**

(c) transferring data between the broadband access devices during the repeating bus frame **[col. 4, lines 1-4];** and

(d) asserting a first control line when valid data from one of the asynchronous data streams appears in a slot of the repeating bus frame **[the LSU is interpreted as asserting the first control line; byte status signals (such as PRSTAT and PXSTAT) are sent from each LSU (via Fig. 1a's PCM control signal 104, col. 6, lines 10-13) wherein each LSU gets two clock cycles to request to transmit an ATM cell, col. 11, lines 31-33; the HSU receives the request and, as the bus master, allows the LSU to transmit (inherently signaled via Fig. 1a's PCM control signal 104, col. 6, lines 10-13), col. 11, lines 39-42].**

9. With regard to claim 13, Gorshe et al. discloses

(e) asserting a second control line at the first slot of the repeating bus frame **[this is interpreted as the HSU, as the bus master (col. 11, lines 39-42), granting the LSU data bus access; this grant is inherently signaled via Fig. 1a's PCM control signal 104 (col. 6, lines 10-13); Fig. 5, the byte status signal (sent via PCM control signal 104, col. 6, lines 10-13)]**

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indicates the beginning-of-cell on the first slot of the 106 clocks per cell slot necessary to transmit a 53 byte ATM cell (via the data bus), col. 11, lines 25-30].

10. With regard to claim 14, Gorshe et al. discloses

(e) asserting a second control line when a slot of the repeating bus frame includes a framing signal of an asynchronous data stream **[this is interpreted as the HSU, as the bus master (col. 11, lines 39-42), granting the LSU data bus access; this grant is inherently signaled via Fig. 1a's PCM control signal 104 (col. 6, lines 10-13); Fig. 5, the byte status signal (sent via PCM control signal 104, col. 6, lines 10-13) indicates the beginning-of-cell on the first slot of the 106 clocks per cell slot necessary to transmit a 53 byte ATM cell (via the data bus), col. 11, lines 25-30].**

Allowable Subject Matter

11. Claims 2, 3, 6, 11, 12 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for

The Examiner has not found a system that transfers synchronous and asynchronous data via time division multiplexed bus system with repeating bus frames that use either (a) 336 slots using a 25 MHz clock signal or (b) 1008 slots using a 75 MHz clock signal.

Response to Arguments

13. Applicant's arguments filed July 10, 2006 have been fully considered but they are not persuasive. Applicant's representative argues that, with respect to claims 1, 4, 5, 7, 9, 10, 13, and 14, Gorshe et al. does not disclose, teach, or suggest asserting at least one control line when valid asynchronous data is present in one of the repeating asynchronous data stream slots in the repeating frames [**Applicant's Response dated July 10, 2006, page 2, line 11 to page 3, line 13**]. Specifically, that Gorshe et al. discloses, teaches, or suggests that cell slot requests are made before asynchronous data appears in a slot and not when the data appears in the slot [**Applicant's Response dated July 10, 2006, page 3, lines 10-13**]. The examiner respectfully disagrees.

14. As noted above, the LSU is interpreted as asserting the first control line; byte status signals (such as PRSTAT and PXSTAT) are sent from each LSU (via Fig. 1a's PCM control signal 104, col. 6, lines 10-13) wherein each LSU gets two clock cycles to request to transmit an ATM cell [**col. 11, lines 31-33**]; the HSU receives the request and, as the bus master, allows the LSU to transmit (inherently signaled via Fig. 1a's PCM control signal 104, col. 6, lines 10-13) [**col. 11, lines 39-42**]. Thus, the interpreted control line is asserted when the asynchronous data appears in the asynchronous data slot of the repeating frame because such a scheme is necessary with the master/slave relationship disclosed in Gorshe et al. with respect to high speed units [HSUs] and low speed units [LSUs].

15. Applicant's representative argues that the cell requests in Gorshe et al. are made before asynchronous data appears in the slot [**Applicant's Response dated July 10, 2006, page 3, lines 10-13**]. The examiner respectfully disagrees. First, it is the examiner's position that asynchronous data must *necessarily* be present before an LSU requests a time slot to load asynchronous data—it would be a waste of timeslots in an arbitrated master/slave scheme to request a timeslot for asynchronous data transmission with no asynchronous data present. Second, the LSUs perform both reception and transmission [**abstract**]. The timeslots allocated for reception are known to the LSUs [*See Id.*]. Thus, when receiving data, a control signal must *necessarily* be asserted in order to *load* asynchronous data onto the arbitrated bus in the master/slave scheme in order for the correct LSU to receive/retrieve the asynchronous data. Third, for transmission, multiple LSUs have asynchronous data appearing in several slots for the many possible LSUs [**col. 11, lines 30-33**]. Each LSU arbitrates for the slots to send the asynchronous data over the bus[es]. Thus, the control signal is asserted when the asynchronous data is already in the slot—in order to allow the data to be put onto the repeating frame [STS-1 traffic].

16. Alternatively, recall that the asynchronous data appears in repeating slots/frames. Thus, for multiple asynchronous data cells, the control signal can be asserted after the first asynchronous data cell—just in time for the second asynchronous data cell to be transmitted/received. The control line does not have to be asserted for the same asynchronous data cell—it can be asserted the next cell or frame afterwards. Additionally, that first asynchronous data cell could belong to

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[or be addressed to] a first LSU. Thus, asynchronous data would already be present in the repeating frame when a second LSU asserts the control signal.

Conclusion

17. Accordingly, **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

18. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Mais whose telephone number is 572-272-3138. The examiner can normally be reached on M-Th 5am-4pm.

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20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MAM
July 19, 2006

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